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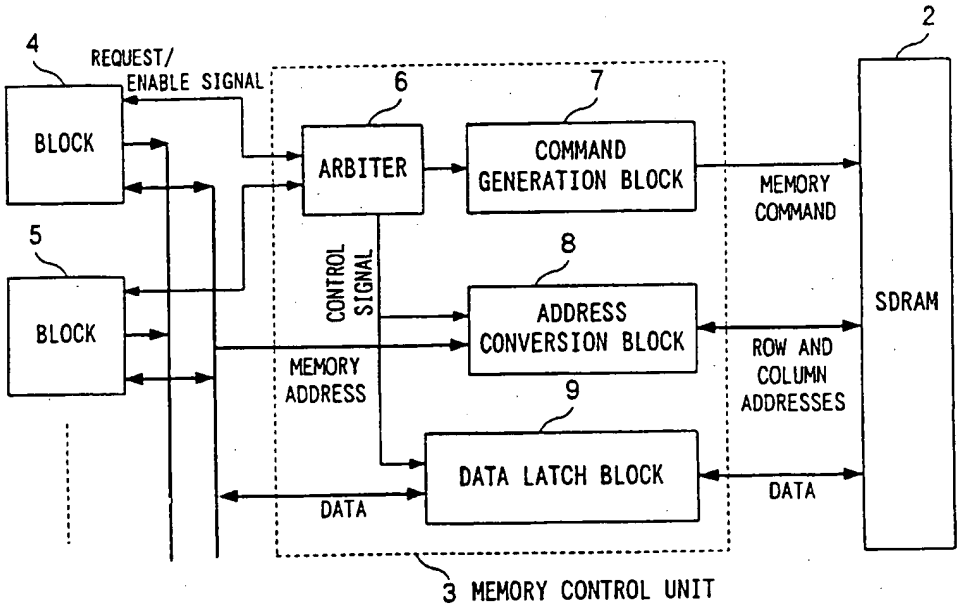

(57) Abstract

To provide a memory control unit which prevents continuous accesses to the same bank of SDRAM to increase its processing speed. The memory control unit (3) of the present invention controls SDRAM (2) which has two banks 0, 1 and can be continuously accessed in multiple-bank mode in which address inputs to the banks 0, 1 are seamlessly alternated between the banks by precharging the banks individually. The memory addresses provided by a block (4, 5) accessing the SDRAM (2) through the memory control unit (3) are converted into addresses such that the memory addresses are input to the banks of the SDRAM (2) alternately.

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DESCRIPTION

MEMORY CONTROL UNIT

Field of the Invention

The present invention relates to a memory control unit for controlling a Synchronous Dynamic Random Access Memory (hereinafter abbreviated as "SDRAM").

Background of the Invention

Recently, SDRAM has come into use which allows burst mode data transfer of cache memory frequently used in personal computers to be performed at high speed synchronized with the clock speed. The SDRAM allows for switching between multiple-bank continuous access mode and random access mode. In the multiple-bank mode, two banks, bank 0 and bank 1 are used. The most significant bit (MSB) of the memory addresses of bank 0 is "0," whereas the MSB of the memory addresses of bank 1 is "1." Bank 0 and bank 1 are accessed alternately by controlling the clock so that data in one of the banks can be read while a memory address for the other bank is obtained.

Memory control unit for controlling the SDRAM, for example those described in, for example, Japanese Patent Laid-Open No. 8-111090 and Japanese Patent Laid-Open No. 8-212170, are known.

The memory control unit 11 for controlling SDRAM described in Japanese Patent Laid-Open No. 8-212170 comprises memory control means 12 and arbitration/wait signal generation means 13 as shown in FIG. 8 and controls accesses to a number of blocks 14 to 17 of the SDRAM 2.

A memory address signal (MADD), a data signal (DATA), and a read/write control signal (RD/WR) are input respectively into memory control parts 18a to 18d corresponding to the respective blocks 14 to 17.

A memory access request signal (CS) from each block 14 to 17 is input into the arbitration/wait signal generating means 13 and from which a wait signal (Wait) is returned to each block 14 to 17.

The memory control part corresponding to the block which received a memory access enable signal (Enable) from the arbitration/wait signal generation means 13 controls the access to the SDRAM2 from the enabled block.

An example of the read access timing for SDRAM 2 using the memory control unit 11 will be described below. In this example, it is assumed that SDRAM2 uses multiple-bank mode.

Bank 0 is selected when the MSB of a memory address provided by a block is "0," whereas bank 1 is selected when the MSB is "1."

As shown in FIG. 9, the row address R0/column addresses C0 pair of bank 0 and the row address R1/column address C1 pair of bank 1 are alternately taken into the SDRAM according to the clock CK. Data D00 and D01 of bank 0 are output at a clock timing at which row address R1 and column address C1 of bank 1 are input. D01 is data which has an address following the address of D00. This means that the two-word data can be output by one address input. When only one-word of data is required, data D01 is not required.

The precharging of each bank is automatically performed at a time point at which the last data, that is, data D01 of two-word data is output. The same applies the precharging of bank 1.

In this way, bank 0 and bank1 of the SDRAM are accessed alternately and seamlessly.

For the memory control unit of the conventional art, in the case where SDRAM uses multiple-bank mode and a single block makes access to the SDRAM, bank 0 is continuously accessed if memory addresses for continuously accessing the same bank (for example, bank is set to 0) is continuously output from

the single block. In such a case, no address can be output to bank 0 until the precharge operation on bank 0 ends. That is, there will be a wasted in which the SDRAM cannot be accessed.

One solution to the problem may be to generate memory addresses in a single block if that single bank accesses the SDRAM so as to access bank 0 and bank 1 alternately. However, it is extremely difficult to correlate memory addresses provided from a plurality of blocks if the plurality of blocks access the SDRAM. Accordingly, the same bank can be continuously accessed because the memory addresses from the blocks are not correlated with each other.

For example, when block B attempts to access block 0 immediately after block A accesses block 0, the same block, (block 0) is continuously accessed. No address can be provided to bank 0 until the precharge operation on bank 0 ends. This means that there is a wasted cycle in which the SDRAM cannot be accessed.

An object of the present invention is to provide a memory control unit for preventing continuous accesses to the same bank of SDRAM to increase its processing speed.

Disclosure of the Invention

The memory control unit of the present invention is arranged so as to convert memory addresses provided from blocks into addresses such that the address inputs are alternated between the banks of the SDRAM.

According to the present invention, a memory control unit is provided which prevents continuous accesses to the same bank of SDRAM to increase its processing speed.

The present invention provides a memory control unit for controlling SDRAM which has a plurality of banks and allows for continuous access in multiple-bank mode in which address inputs to the banks are seamlessly alternated between the

banks of the SDRAM by precharging the banks individually, wherein the memory control unit is arranged so as to convert memory addresses from a block accessing to the SDRAM through the memory control unit into addresses such that the addresses are input to the banks of the SDRAM alternately. The memory addresses from the blocks are converted so as to be able to be input to the banks alternately between them even if the memory addresses which would otherwise cause continuous accesses to the same bank of the SDRAM are provided by the blocks, thus the banks can be accessed always alternately. Therefore, a useless cycle in which the SDRAM cannot be accessed is eliminated, and commands can be continuously issued to the SDRAM to increase its processing speed. From the viewpoint of the blocks generating memory addresses, they can generate the memory addresses without paying attention to the banks.

The present invention further provides a memory control unit for controlling SDRAM which is divided into at least two banks and allows for switching between multiple-bank continuous access mode and random access mode, said multiple-bank continuous access mode enabling address inputs to the banks to be seamlessly alternated by precharging the banks individually, characterized in that the memory control unit comprises an arbiter for arbitrating memory access requests from a plurality of blocks accessing the SDRAM through the memory control unit, a command generation block for generating a memory command to be issued to the SDRAM, an address conversion block for converting memory addresses from a block to which access right is given by the arbiter into row and column addresses so that the addresses are input to the banks of the SDRAM alternately, a data latch block for latching write data from a block to which access right is given by the arbiter or read data from the SDRAM to pass the data between the block and the SDRAM. Even if memory addresses

provided by the plurality of blocks are not correlated with each other, the same bank of the SDRAM is not continuously accessed, memory access in multiple-bank mode is easily assured, and commands can be continuously issued to the memory, resulting in increased processing speed.

The present invention further provides a memory control unit for controlling SDRAM by pairing memory access units provided by each block in the respective banks so that the banks of the SDRAM are alternately accessed. A same single bank of the SDRAM is not continuously accessed and a plurality of banks are accessed alternately.

The present invention further provides a memory control unit, wherein the command generation block is arranged to generate a mask signal for disabling access data corresponding to an excess or deficiency of memory access from the block in the SDRAM if the memory access units provided by the block to which access right is given are not paired in the respective banks. This eliminates the need for controlling a number of signals or re-specifying a burst length, which would be necessary in the conventional art. The memory access can be controlled simply by using the mask signal without changing the memory access units of the banks, resulting in simplified circuitry for memory control.

Brief Description of the Drawings

FIG. 1 is a block diagram showing the configuration of a memory control unit according to embodiment 1 of the present invention;

FIG. 2 is a diagram for describing address conversion in an address conversion block according to embodiment 1 of the present invention;

FIG. 3 is a timing diagram showing the timing of accessing to each bank according to embodiment 1 of the present invention;

FIG. 4 is a diagram for describing an example of address conversion which is different from embodiment 1;

FIG. 5 is a diagram for describing an example of address conversion which is different from embodiment 1;

FIG. 6 is a timing diagram showing a memory access unit for each block according to embodiment 2 of the present invention;

FIG. 7 is a timing diagram showing different memory access units according to embodiment 3 of the present invention;

FIG. 8 is a block diagram showing a configuration of a memory control unit according to a conventional art; and

FIG. 9 is a timing diagram showing the timing of accessing to each bank according to the conventional art.

A memory control unit according to the present invention will be described below with respect to specific embodiments.

Embodiments

(Embodiment 1)

A memory control unit according to embodiment 1 shown in FIG. 1 controls SDRAM 2 having two banks 0, 1 and allowing for continuous access in multiple-bank mode in which address inputs are seamlessly alternated between banks 0 and 1 by precharging the banks individually as in the conventional art. Unlike the conventional art, the memory control unit of embodiment 1 is arranged to convert memory addresses provided by blocks 4, 5 accessing SDRAM 2 through the memory control unit 3 as shown in FIG. 1 into addresses such that the converted addresses are input to bank 0 and bank 1 alternately.

As shown in FIG. 1, the memory control unit 3 comprising an arbiter 6 for arbitrating memory access requests from the plurality of blocks 4, 5 accessing the SDRAM 2, a command generation block 7 for generating a memory command to the SDRAM 2, an address conversion block 8 for converting memory addresses from a block to which access right is given by the

arbiter 6 into row and column addresses such that the addresses are input to the banks of the SDRAM 2 alternately, a data latch block 9 for latching write data from a block to which access right is given by the arbiter 6 or read data from the SDRAM 2 to pass the data between the block and the SDRAM 2.

The blocks 4, 5 may be a computer which, for example, transfers data between a host computer and a microcomputer through SDRAM 2, or may be an error correction block which corrects erroneous data.

Operations of the memory control unit 3 for writing data from the block 4 into the SDRAM 2 in multiple-bank mode will be described below.

Here, it is assumed that the SDRAM 2 is programmed for a burst length of "2," that is, when an address is specified, two wards of data, one for the specified address and one for the succeeding address, are accessed.

When the block 4 accesses the SDRAM 2, an address, data, and a control signal are provided to the SDRAM 2 through the memory control unit 3.

The block 4 outputs a write request signal to the arbiter 6 of the memory control unit 3.

The arbiter 6 returns an enable signal to the block 4 if no other block is accessing the SDRAM 2, or returns an enable signal to a block having a higher priority if the block 5 also outputs a request signal simultaneously with the block 4. In this example, it is assumed that the block 4 has the highest priority and enabled to access to the SDRAM 2 by the arbiter 6.

The arbiter 6 directs the address conversion block 8 to obtain the memory address output from the enabled block 4, and directs the data latch block 9 to obtain the data to be written output from the block 4. At the same time, it directs the command generation block 7 to generate memory commands,

including Row Address Strobe (RAS) and Column Address Strobe (CAS).

The address conversion performed in the address conversion block 8 will be described below.

The address conversion block 8 converts the memory addresses received from the block 4 into addresses such that the converted addresses are input to bank 0 and bank 1 of the SDRAM 2 alternately.

Because the SDRAM 2 is programmed for a burst length of "2," the memory address is incremented by two as it is output from the block 4, as shown in FIG. 2(a). The MSB of the memory address indicates a bank address. If the MSB is "0," then bank 0 would be selected and if it is "1," then bank 1 would be selected. Thus, bank 0 of the SDRAM 2 would be selected continuously because the MSBs of all the memory addresses before conversion shown in FIG. 2 (a) are "0" unless they are otherwise changed.

Therefore, the second bit from the least significant bit (LSB) of each of the memory addresses before conversion shown in FIG. 2(a) is made to the MSB of the converted memory address, and the bits higher than a third bit before conversion is shifted toward the LSB by one bit, generating the converted memory address as shown in FIG. 2(b).

As shown in FIG. 2(b), the MSBs of the resulting memory addresses alternate between 0 and 1. Thus, bank 0 and bank 1 are always accessed alternately and the each block can generate memory addresses without taking care of the banks.

In this way, the address conversion block 8 performs memory address conversion and generates row and column addresses based on the converted memory addresses shown in FIG. 2(b) to output them to the SDRAM 2.

The data latch block 9 outputs each latched write data to the SDRAM 2 and the command generation block 7 outputs the memory commands mentioned above to the SDRAM 2.

Now, the access timing to each bank of the SDRAM 2 will be described below.

As shown in FIG. 3, row address R00 and column address C00 of bank 0 and row address R10 and column address C10 of a bank 1 are alternately obtained according to the clock CK. Data D00, D01 of bank 0 are output at clock timing at which row address R10, column address C10 of the bank 1 are input. D01 is data of the address following D00. This means that two words of data can be output by one address input. The precharge of each bank is automatically performed at a timing at which the last data, that is, data D01, D11, D03 ... of two-word data is output. The same applies to the precharging of bank 1.

Because of this arrangement, the memory addresses from the blocks can be converted so as to be input to the banks alternately even if memory addresses which would otherwise cause continuous access to the same bank of the SDRAM 2 are output from the blocks, thus preventing continuous access to the same bank. That is, the banks can be accessed always alternately, so that a wasted cycle in which the SDRAM 2 cannot be accessed is eliminated and commands can be continuously issued to the SDRAM 2 to increase its processing speed. From the viewpoint of the blocks generating memory addresses, the memory addresses can be generated without taking care of the banks.

In the description of embodiment 1, the SDRAM 2 programmed for a burst length of "2" has been described by way of example. If the SDRAM 2 is programmed for a burst length of "4" for example, the third bit from the LSB of a memory address before conversion shown in FIG. 4(a) is made to the MSB of the converted memory address shown in FIG. 4(b) and the bits higher than the fourth bit from the LSB of the memory address before conversion are shifted by one bit toward the lower bits to generated the converted memory address as shown in FIG. 4(b).

If the SDRAM 2 is programmed for a burst length of "1," the LSB of a memory address before conversion shown in FIG. 5(a) is made to the MSB of the converted memory address shown in FIG. 5(b), and the bits higher than the second bit from the LSB of the memory address before conversion shown in FIG. 5(a) are shifted by one bit toward the lower bits, thus generating the converted memory address as shown in FIG. 5(b).

(Embodiment 2)

A memory control unit according to embodiment 2 of the present invention is similar to embodiment 1 described above, except that a feature is added to the memory control unit 3 of the embodiment 1 for pairing different banks as a unit for accessing by each block 4, 5 so that bank 0 and bank 1 are accessed alternately with each other to control the SDRAM 2.

The memory control unit 3 controls the SDRAM 2 by pairing bank 0 and bank1 as a memory access unit accessed by each block so that the banks are alternately accessed. For example, if the SDRAM 2 is programmed for a burst length of "2" in multiple-bank mode, the access unit of each block 4, 5 is four words so that each block uses two words for bank 0 and two words for bank 1 as a pair.

Here, operations of the memory control unit 3 will be described in the case where a plurality of blocks (for example blocks 4, 5) access the SDRAM 2 in multiple-bank mode to write data from the blocks 4, 5 into the SDRAM 2. The SDRAM 2 is assumed to be burstlength "2" mode.

Since the process is the same as embodiment 1 described above to the point where data from the command generation block 7, the address conversion block 8, and the data latch block 9 are output to the SDRAM 2, the description of which will be omitted here.

Even if the block 5 accesses the SDRAM 2 immediately after the block 4 accesses the SDRAM 2 as shown in FIG. 6, the accesses are always alternated between bank 0 and bank 1 at the point

of switching from the block 4 to block 5, because each block accesses four words as a unit by pairing two-word data for bank 0 and two-word data for bank 1.

Thus, because of such a configuration even if the plurality of blocks 4, 5 access the SDRAM 2 and the memory addresses from the plurality of blocks 4, 5 are not correlated with each other, continuous accesses to the same bank of the SDRAM 2 are prevented. That is, the banks are always accessed alternately, the generation of wasteful cycle which cannot access to the SDRAM 2 can be eliminated, and commands can be issued to the SDRAM 2 continuously, resulting in increased processing speed.

(Embodiment 3)

A memory control unit 3 according to embodiment 3 of the present invention is similar to that of embodiment 2 described above, except that a feature is added to the command generation block 7 of embodiment 2 for generating and outputting a mask signal which, if the memory access from the block is not to a pair of different banks, disables excess or short memory access data provided by a block to which access right is given in the SDRAM 2.

Here, operations of the memory control unit 3 in the case where the block 4 accesses only bank 0 of the SDRAM 2 in multiple-bank mode and block 5 accesses bank 0 and bank 1 continuously to write data from the blocks 4, 5 into the SDRAM 2, as shown in FIG. 7. The SDRAM2 is assumed to be in burstlength "2" mode.

The block 4 accesses two words as a unit, which is less than the memory access unit (four words) in embodiment 2 described above.

Whether a random address is accessed or data is accessed in two words as a unit by the block 4 as shown in FIG. 7(b), the memory control unit 3 issues a memory command (WRITE) and addresses (R10, C10) corresponding to bank 1.

When a write operation is performed in this example, the command generation block 7 generates a mask signal which disables write data (D10, D11), which is short access data from the block 4, in the SDRAM 2.

The write data (D10, D11) shown in FIG. 7(b) may be any other value.

The SDRAM 2 does not write data (D10, D11) in the interval in which the mask signal is high.

In the conventional art, memory commands, including RAS and CAS and addresses, must be controlled so as not to be issued, that is, the memory command (WRITE) and the addresses (R10, C10) must be controlled not to be issued, as shown in FIG. 7(a). Because memory commands are combination of a number of signals (/CS, /RAS, /CAS, /WE, and addresses) provided to the SDRAM 2 and all of these signals must be controlled or the burst length of the SDRAM 2 must be re-specified, the circuitry becomes considerably complicated in the conventional art. On the contrary, the memory control unit 3 according to embodiment 3 eliminates the need for controlling a number of signals or re-specifying a burst length. The control can be simplified because it is accomplished by simply using the mask signal without changing the memory access unit. Accordingly the circuitry can be simplified.

While in the description of the embodiments above operations for writing data from a block to the SDRAM 2 have been described, the similar effects can be obtained in the case where data read out from the SDRAM 2 is output to the block.

CLAIMS

1. A memory control unit for controlling SDRAM (2) which has a plurality of banks and allows for continuous access in multiple-bank mode in which address inputs to said banks are seamlessly alternated by precharging said banks individually, characterized in that

memory addresses provided by blocks (4, 5) accessing said SDRAM (2) through said memory control unit (3) are converted so that the addresses are input into the respective banks of the SDRAM (2) alternately.

2. A memory control unit (3) for controlling SDRAM (2) internal of which is divided into at least two banks and allows for switching between a multiple-bank continuous access mode and a multiple-bank random access mode, said multiple-bank continuous access mode enabling address inputs to said banks to be seamlessly alternated by precharging said banks individually, characterized by comprising:

an arbiter (6) for arbitrating memory access requests from a plurality of blocks (4, 5) accessing said SDRAM (2) through said memory control unit (3);

a command generation block (7) for generating a memory command to said SDRAM (2);

an address conversion block (8) for converting memory addresses from a block (4, 5) to which access right is given by said arbiter (6) into row and column addresses so that the addresses are input to the banks of said SDRAM (2) alternately and output from said SDRAM (2); and

a data latch block (9) for temporarily latching write data provided by a block (4, 5) to which access right is given by said arbiter (6) or read data from said SDRAM (2) in order to pass the data between the block (4, 5) and said SDRAM (2).

3. The memory control unit according to claim 2, characterized in that said SDRAM (2) is controlled by pairing memory access units provided by each block (4, 5) in the respective banks so that the banks are alternately accessed.

4. The memory control unit according to claim 2, characterized in that the command generation block (7) is arranged to generate a mask signal for disabling access data corresponding to an excess or deficiency of memory access from the block (4, 5) in said SDRAM (2) if the memory access units provided by the block (4, 5) to which the access right is given are not paired in the respective banks.

Fig. 1

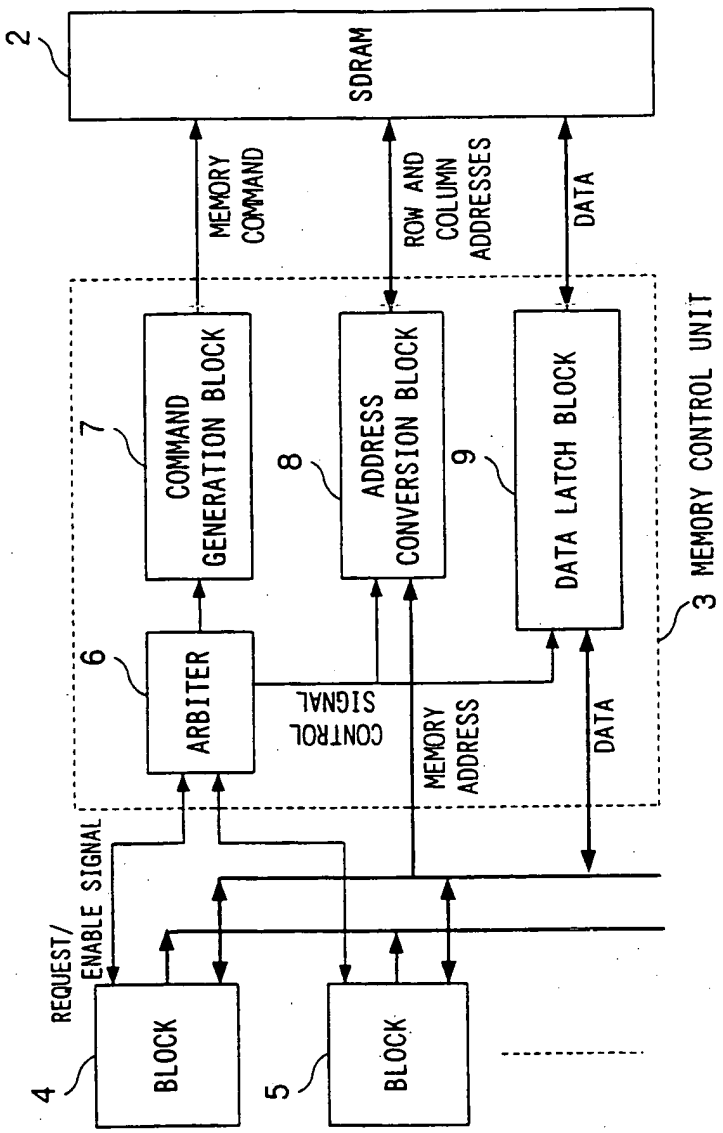

2
SDRAM
MEMORY COMMAND
ROW AND COLUMN ADDRESSES
DATA
3 MEMORY CONTROL UNIT
7
COMMAND GENERATION BLOCK
8
ADDRESS CONVERSION BLOCK
9
DATA LATCH BLOCK
6
ARBITER
CONTROL SIGNAL
MEMORY ADDRESS
DATA
REQUEST/ ENABLE SIGNAL
4
BLOCK
5
BLOCK

Fig. 2

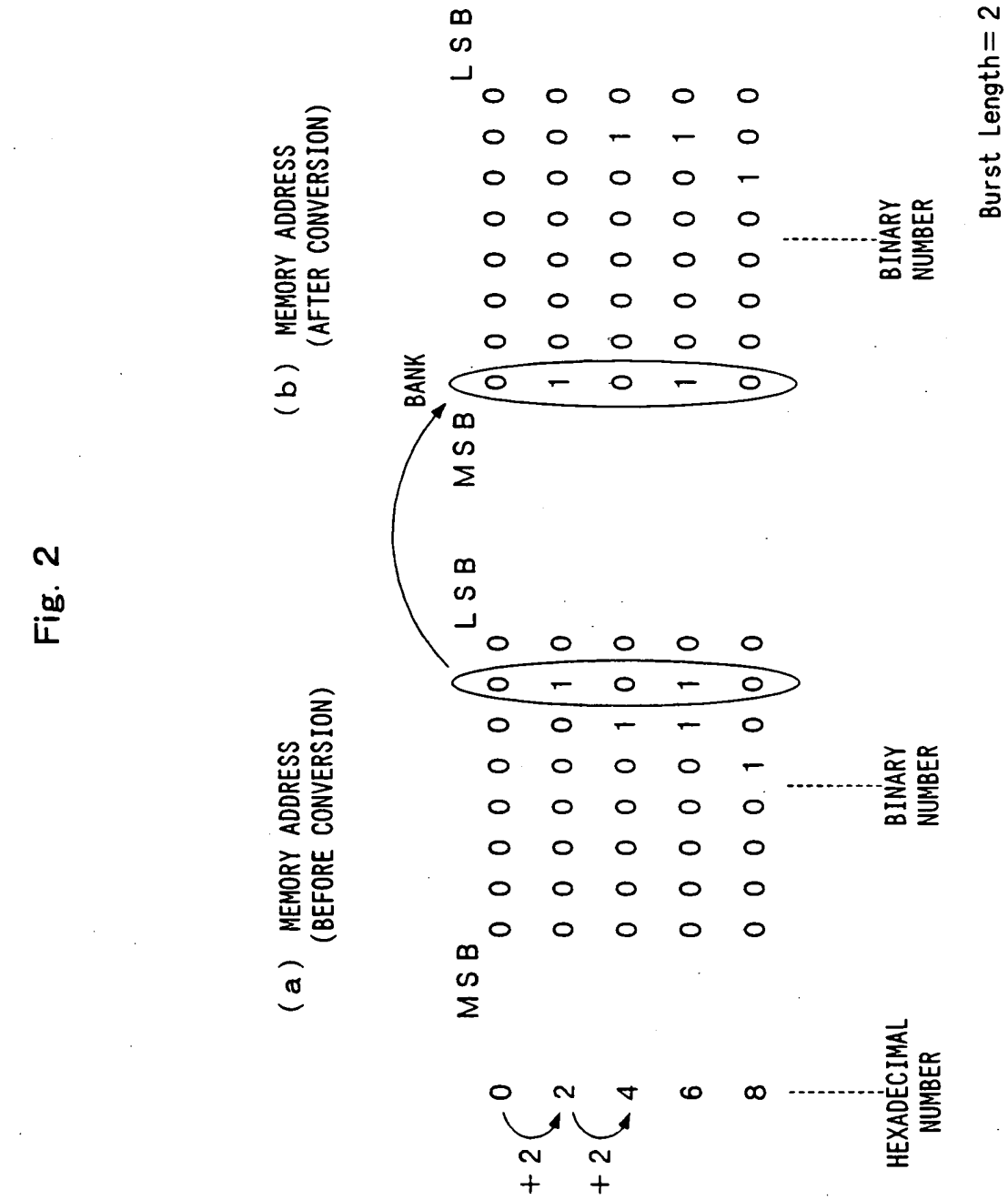

(a) MEMORY ADDRESS (BEFORE CONVERSION)
(b) MEMORY ADDRESS (AFTER CONVERSION)
MSB
LSB
BANK
BINARY NUMBER
HEXADECIMAL NUMBER
+2
+2
0
2
4
6
8
Burst Length=2

Fig. 3

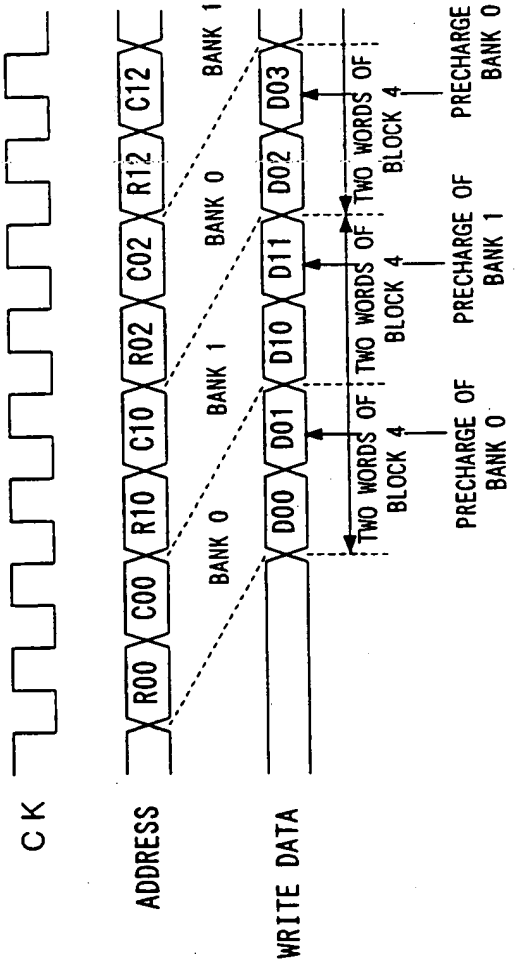

CK
ADDRESS
WRITE DATA
R00
C00
R10
C10
R02
C02
R12
C12
D00
D01
D10
D11
D02
D03
BANK 0
BANK 1
BANK 0
BANK 1
TWO WORDS OF BLOCK 4
TWO WORDS OF BLOCK 4
TWO WORDS OF BLOCK 4
PRECHARGE OF BANK 0
PRECHARGE OF BANK 1
PRECHARGE OF BANK 0
Burst Length = 2
CAS Latency = 2

Fig. 4

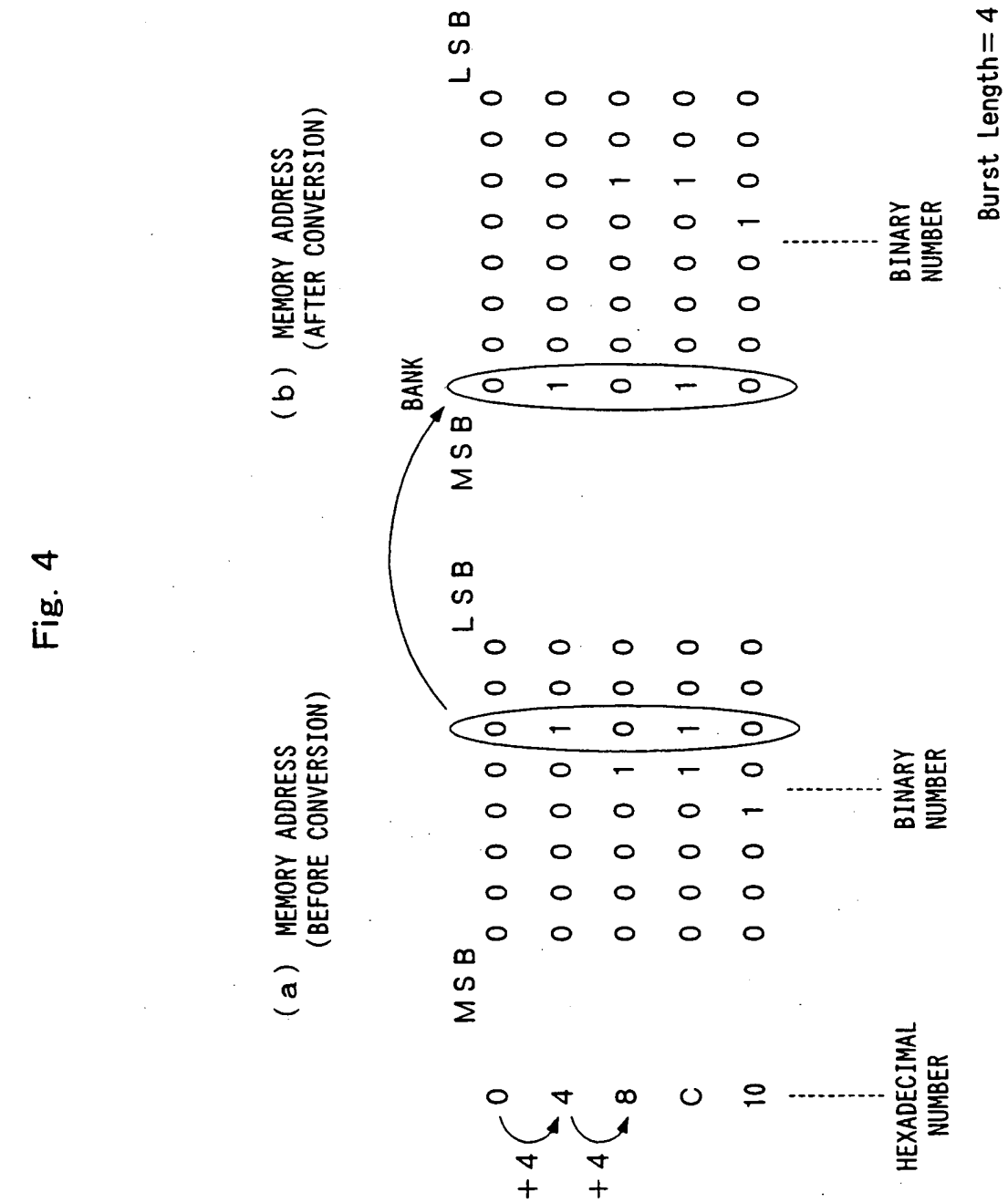

(a) MEMORY ADDRESS (BEFORE CONVERSION)
(b) MEMORY ADDRESS (AFTER CONVERSION)
MSB
LSB
BANK
BINARY NUMBER
HEXADECIMAL NUMBER
0
4
8
C
10
+4
+4
Burst Length=4

Fig. 5

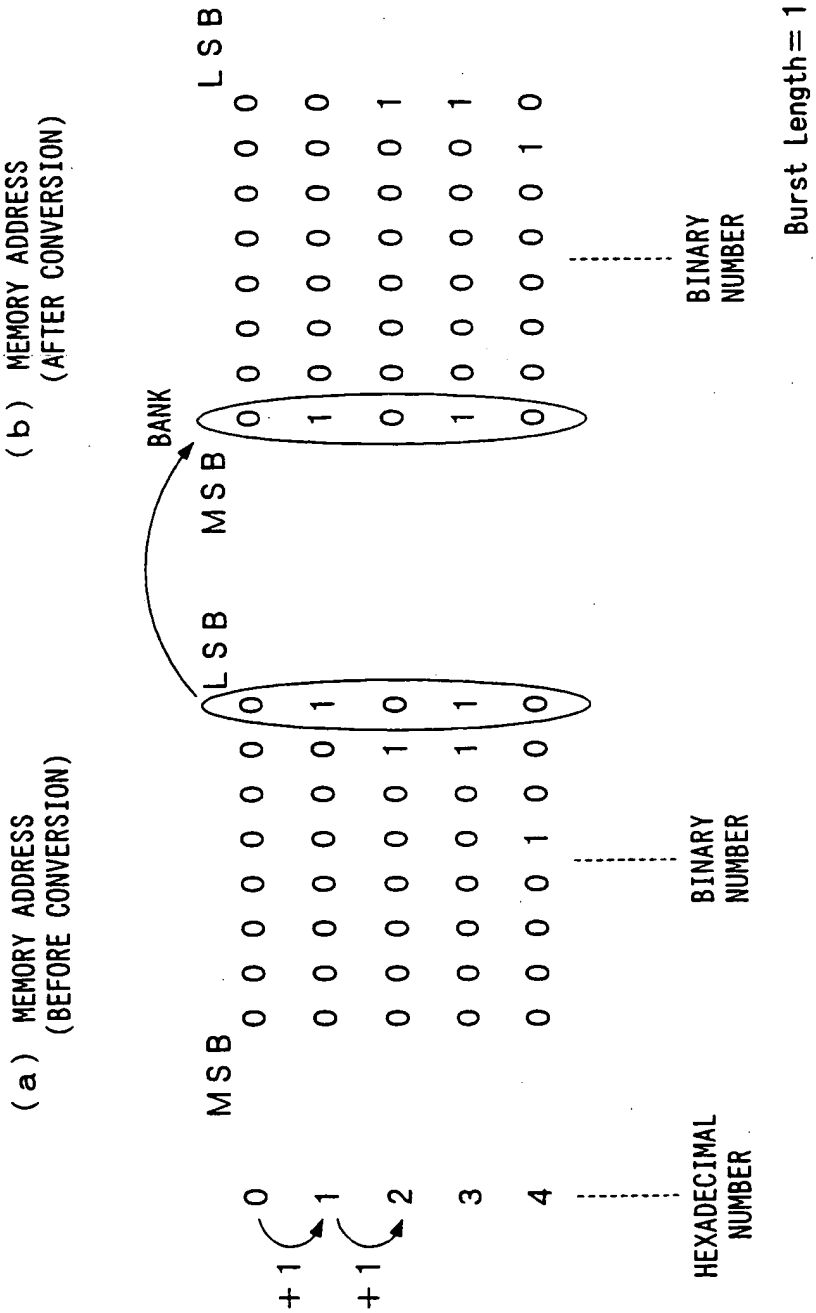

(a) MEMORY ADDRESS (BEFORE CONVERSION)
(b) MEMORY ADDRESS (AFTER CONVERSION)
MSB
LSB
BANK
HEXADECIMAL NUMBER
BINARY NUMBER
BINARY NUMBER
Burst Length= 1
+1
+1

Fig. 6

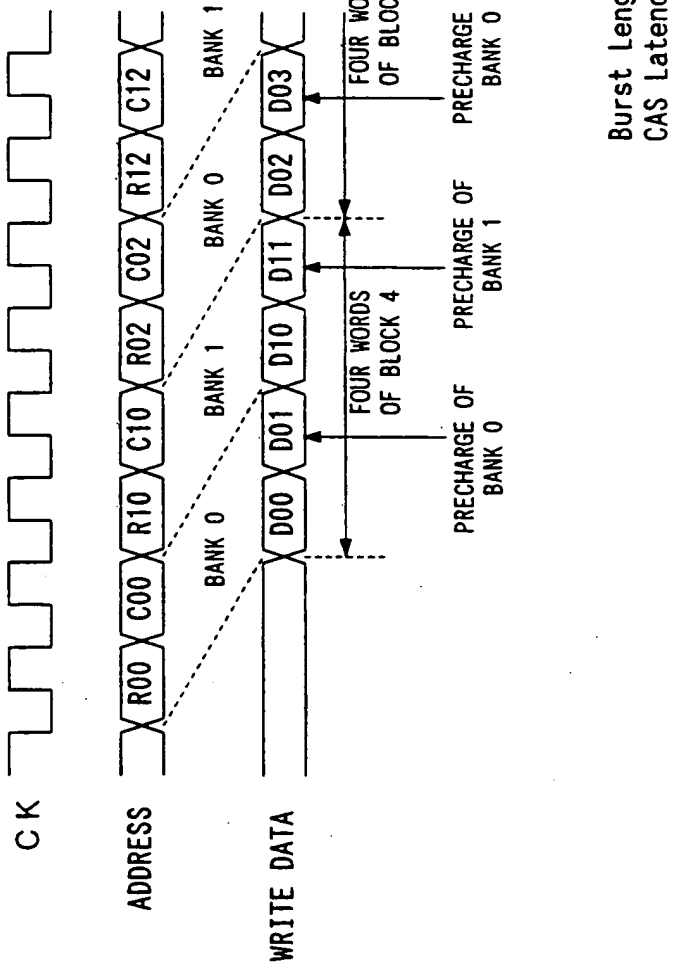

CK
ADDRESS
WRITE DATA
R00
C00
R10
C10
R02
C02
R12
C12
D00
D01
D10
D11
D02
D03
BANK 0
BANK 1
BANK 0
BANK 1
FOUR WORDS OF BLOCK 4
FOUR WORDS OF BLOCK 5
PRECHARGE OF BANK 0
PRECHARGE OF BANK 1
PRECHARGE OF BANK 0
Burst Length = 2
CAS Latency = 2

Fig. 7

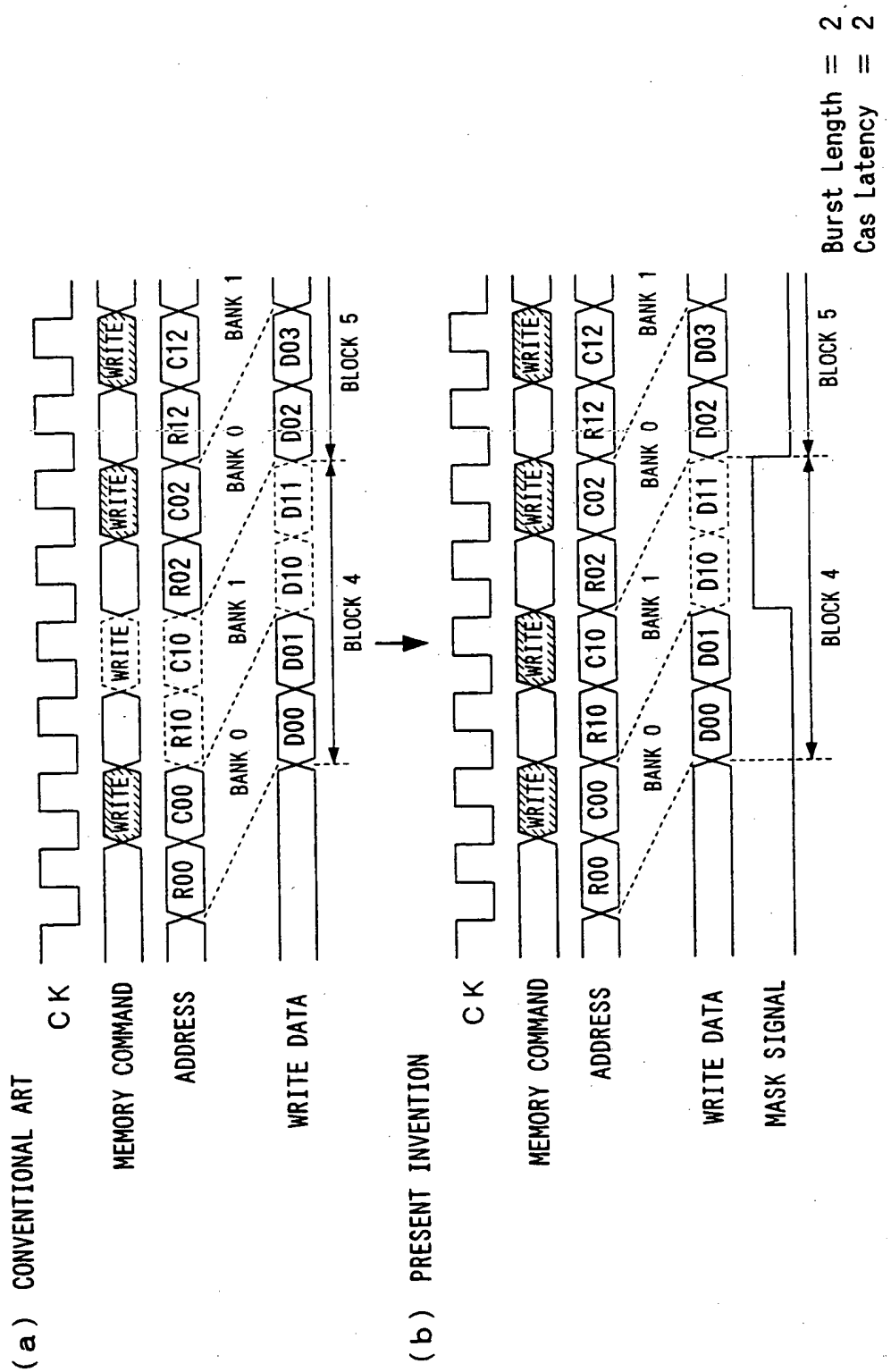


Fig. 8

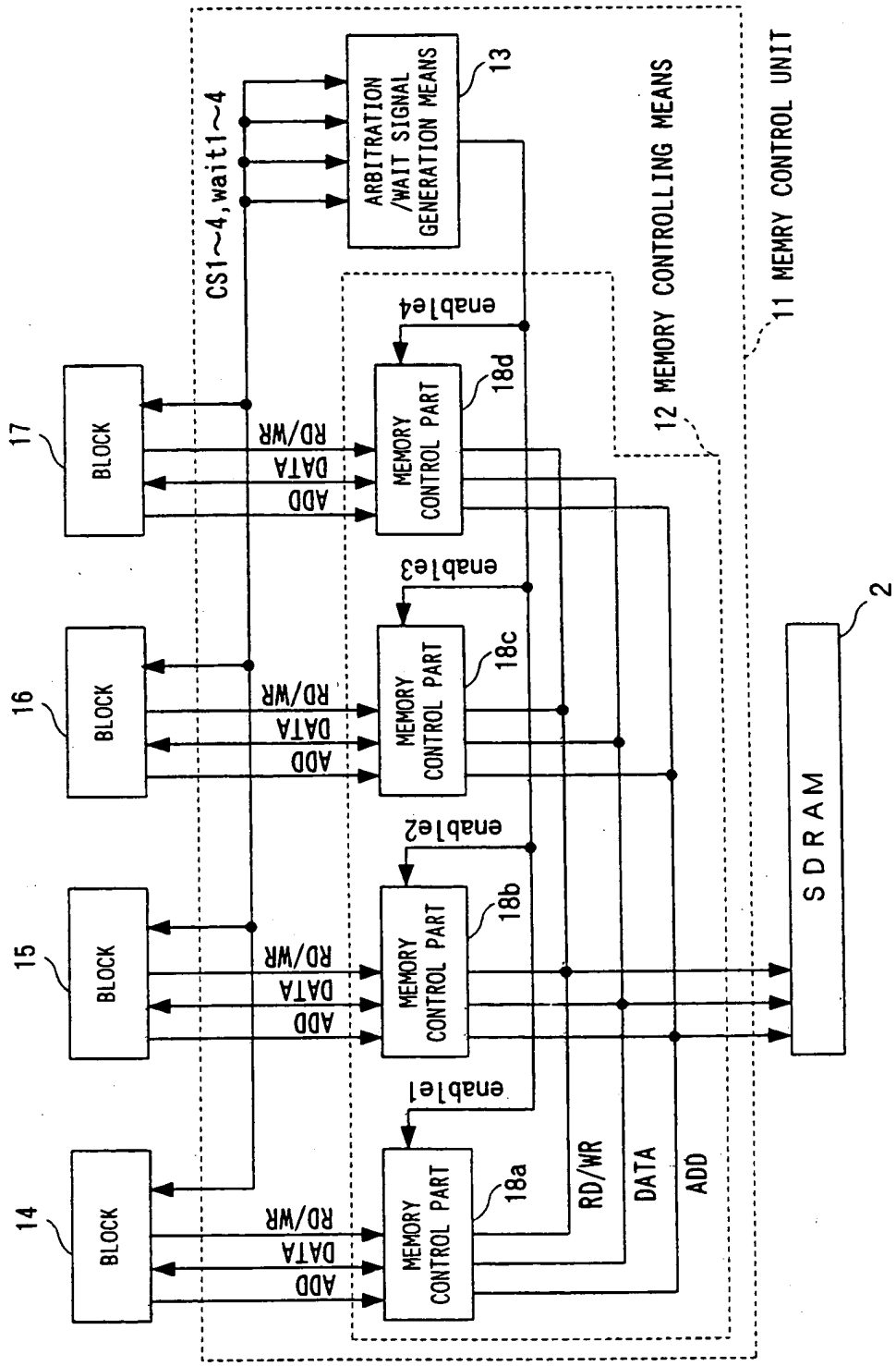
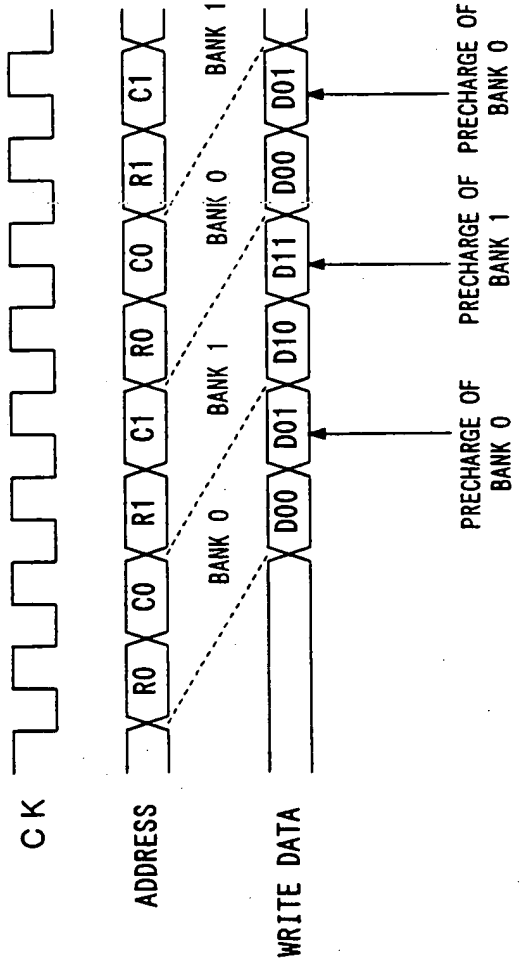

11 MEMRY CONTROL UNIT
12 MEMORY CONTROLLING MEANS
ARBITRATION /WAIT SIGNAL GENERATION MEANS
13
CS1~4, wait1~4
enable4
enable3
enable2
enable1
MEMORY CONTROL PART
18d
18c
18b
18a
BLOCK
17
16
15
14
RD/WR
DATA
ADD
RD/WR
DATA
ADD
SDRAM
2

Fig. 9


CK
ADDRESS
WRITE DATA
R0
C0
R1
C1
R0
C0
R1
C1
D00
D01
D10
D11
D00
D01
BANK 0
BANK 1
BANK 0
BANK 1
PRECHARGE OF BANK 0
PRECHARGE OF BANK 1
PRECHARGE OF BANK 0

INTERNATIONAL SEARCH REPORT

Inte onal Application No
PCT/JP 00/02654

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F12/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	EP 0 481 597 A (IBM) 22 April 1992 (1992-04-22) column 4, line 2 - line 52; figures 3,4	1,2 3,4
Y	WO 94 08295 A (FLAVORS TECH INC) 14 April 1994 (1994-04-14) page 21, line 27 -page 31, line 14; figure 8; tables 1-4	3,4
X	EP 0 444 601 A (NIPPON ELECTRIC CO) 4 September 1991 (1991-09-04) column 5, line 58 -column 8, line 10; figures 1,2	1,2
A	EP 0 261 751 A (TEKTRONIX INC) 30 March 1988 (1988-03-30) column 5, line 17 -column 7, line 19; figure 1	3

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 July 2000	26/07/2000

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

Information on patent family members

Inte onal Application No
PCT/JP 00/02654

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0481597 A	22-04-1992	US 5226134 A	06-07-1993
		AU 640813 B	02-09-1993
		AU 8345391 A	09-04-1992
		BR 9104142 A	02-06-1992
		CA 2050950 A,C	02-04-1992
		CN 1060731 A,B	29-04-1992
		JP 2019553 C	19-02-1996
		JP 4230547 A	19-08-1992
		JP 7052407 B	05-06-1995
		KR 9513260 B	26-10-1995
		PT 99117 A	29-10-1993
		SG 44360 A	19-12-1997
WO 9408295 A	14-04-1994	AU 5294193 A	26-04-1994
EP 0444601 A	04-09-1991	JP 3248243 A	06-11-1991
		DE 69131734 D	02-12-1999
		DE 69131734 T	08-06-2000
		US 5274788 A	28-12-1993
EP 0261751 A	30-03-1988	JP 63091757 A	22-04-1988
		US 4818932 A	04-04-1989